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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/050,793	01/18/2002	Akihiko Ebina	15.55/6364	9576

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EXAMINER
DICKEY, THOMAS L

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 05/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/050,793	EBINA, AKIHIKO	
	Examiner	Art Unit	
	Thomas L Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2-11 and 15* is/are allowed.

6)☒ Claim(s) *1 and 12-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *14 April 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *11* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The amendment filed on 04/14/03 has been entered.

Drawings

2. Applicant's arguments concerning the drawing objection of paper #7 are found persuasive, and the objection is withdrawn.

The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on 04/14/03 have been approved.

Information Disclosure Statement

3. The Information Disclosure Statement filed on 04/23/03 has been considered.

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The following title is suggested: "NOVEL BiCMOS INVERTER".

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 12,13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over WOLF "Silicon Processing for the VLSI Era" in view of Manning (6,137,146) and SCHWANK et al. (6,268,630).

Wolf discloses a semiconducting device with a semiconductor layer, an element isolation region formed in the semiconductor layer; and a first element forming region and a second element forming region defined by the element isolation region; wherein the first element forming region includes both a first bi-polar transistor Q1 and a first field effect transistor M1; the first bi-polar transistor Q1 includes a first emitter region of a first (n) conduction type, a first base region of a second (p) conduction type, and a first collector region of the first (n) conduction type, the first field effect transistor M1 includes a first gate electrode layer, a source region of the first (n) conduction type, and a drain region of the first (n) conduction type, the first field effect transistor M1 further includes a first body region of the second (p) conduction type formed at least between the source region of the first conduction type and the drain region of the first conduction type, the drain region of the first conduction type is electrically connected to the first collector region of the first conduction type, and the source region of the first conduction type is formed structurally isolated from the first emitter region of the first conduction type, and wherein the second element forming region includes both a second bi-polar transistor Q2 and a second field effect transistor M2, the second bi-polar transistor Q2 includes a

second emitter region of the first (n) conduction type, a second base region of the second (p) conduction type, and a second collector region of the first (n) conduction type, the second field effect transistor M2 includes a second gate electrode layer, a source region of the second (p) conduction type, and a drain region of the second (p) conduction type, the second field effect transistor M2 further including a first body region of the first (n) conduction type formed at least between the source region of the second conduction type and the drain region of the second conduction type, the source region of the second conduction type is electrically connected to the second collector region of the first conduction type, the drain region of the second conduction type is electrically connected to the second base region of the second conduction type, the first collector region of the first conduction type is electrically connected to the second emitter region of the first conduction type, and the first gate electrode layer is electrically connected to the second gate electrode layer. Note figures 7-74(a) (top figure. Note that this figure includes two extra MOSFETS that are not needed to meet the claim) and 7-75(a) of Wolf. Wolf does not disclose an insulation layer upon which the semiconductor layer is formed, or placing the first body region of the second conduction type in contact with and electrically connected to the first base region of the second conduction type, or electrically connecting the first body region of the second conduction type to the source region of the first conduction type, or electrically connecting the first body region of the first conduction type to the second collector region of the first conduction type. Wolf does, however, teach electrically connecting the source region of the first conduction

type to the first base region of the second conduction type (as opposed to electrically connecting both of these regions to the first body region of the second conduction type), and naturally, as stated above as a claim limitation, Wolf teaches that the source region of the second conduction type is electrically connected to the second collector region of the first conduction type. With respect to claims 13 and 14, Wolf does not specifically disclose that the semiconductor layer is a silicon layer, nor does Wolf discuss reversing the conductivity types, making the first type p-type so that the type of the BPT bases, the second type, is n-type.

However, Manning discloses a semiconductor device having an element forming region 18 which includes both a first bipolar transistor and a first field effect transistor. In common with the disclosure of Wolf, Manning shows the first bi-polar transistor includes a first emitter region 36 of a first conduction type, a first base region 26c of a second conduction type, and a first collector region 22 of the first conduction type and the first field effect transistor includes a first gate electrode layer 14f, a source region 40 of the first conduction type, and a drain region 36 (note that the region 36 forms both a drain region and an emitter region 36, just as does region A20 form both drain and emitter in applicant's illustration of an embodiment of the claimed invention) of the first conduction type, the first field effect transistor further includes a first body region 26 of the second conduction type formed at least between the source region 40 of the first conduction type and the drain region 36 of the first conduction type, the first body region 26 of the second conduction type is electrically connected to the source region 40 of the first

conduction type, the drain region 36 of the first conduction type is electrically connected to the first collector region 22 of the first conduction type, and the source region 40 of the first conduction type is formed structurally isolated from the first emitter region 36 of the first conduction type. Furthermore, Manning shows the first body region (which is the part of 26c under the gate 14f) of the second conduction type is in contact with and thereby electrically connected to the first base region (the portion of part 26c formed between emitter 36 and collector 22) of the second conduction type, Note figure 9 and column 6 lines 1-32 of Manning.

Further, Schwank et al. discloses an SOI CMOS transistor including an insulation layer upon which the semiconductor layer is formed, wherein on the right side, the first body region 28 of the second conduction type is electrically connected to the source region 52 of the first conduction type by way of body tie 56 and electrode 58, and wherein on the left side, the first body region 28 of the first conduction type is electrically connected to the source region 52 of the second conduction type by way of the other body tie 56 and the other electrode 58. Note figure 1 of Schwank et al. Therefore, it would have been obvious to a person having skill in the art to augment Wolf's semiconducting device with the insulation layer upon which the semiconductor layer is formed such as taught by Manning in order to increase the transconductance to thus provide faster response and higher frequency operation, and to augment the semiconducting device by electrically connecting the first body region of the second conduction type to the source region of the first conduction type and thus to the first

base region of the second conduction type, and electrically connecting the first body region of the first conduction type to the source region of the second conduction type, and thus to the second collector region of the first conduction type, such as taught by Schwank et al., in order to harden the device against SEU radiation. Also, it would have been obvious to a person having skill in the art to place the first body region of the second conduction type of Wolf's semiconducting device in contact with and electrically connected to the first base region of the second conduction type such as taught by Manning, in order to save space on the surface of the semiconducting device to thus increase the density of the logic circuitry.

With regard to claim 13, the teachings of Wolf, Manning, and Schwank et al., combined, yield a device with two NPN bipolar transistors coupled to a PMOS and an NMOS transistor. This device has all the limitations of the semiconductor device of claim 13 except that in claim 13, with the first type defined as p type, the bipolar transistors are PNP coupled to an NMOS and a PMOS transistor. Although the device yielded by the teachings of Wolf, Manning, and Schwank et al. does not teach the exact type of base, emitter, collector, source, drain, and body conductivities as that claimed by Applicant, the conductivity type differences are considered obvious design choices and are not patentable unless unobvious or unexpected results are obtained from these changes. It appears that these changes produce no functional differences and therefore would have been obvious. Note *In re* Leshin, 125 USPQ 416.

Response to Arguments

5. Applicant's arguments filed 04/14/03 with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

6. Claim 15 is allowed over the references of record for the reasons set forth in paper #7.

7. Claims 2-11 are allowed over the references of record for the following reasons:

As a starting point in the analysis of the allowability of claims 2-11, it is noted that all of these claims require a device that includes an insulation layer; a semiconductor layer formed on the insulation layer; an element isolation region formed in the semiconductor layer; and a first element forming region and a second element forming region defined by the element isolation region; wherein the first element forming region includes both a first bi-polar transistor and a first field effect transistor; the first bi-polar transistor includes a first emitter region of a first conduction type, a first base region of a second conduction type, and a first collector region of the first conduction type, the first field effect transistor includes a first gate electrode layer, a source region of the first conduction type, and a drain region of the first conduction type, the first field effect transistor further includes a first body region of the second conduction type formed at least between the source region of the first conduction type and the drain region of the

first conduction type, the first body region of the second conduction type is electrically connected to the source region of the first conduction type, the first body region of the second conduction type is electrically connected to the first base region of the second conduction type, the drain region of the first conduction type is electrically connected to the first collector region of the first conduction type, and the source region of the first conduction type is formed structurally isolated from the first emitter region of the first conduction type, and wherein the second element forming region includes both a second bi-polar transistor and a second field effect transistor, the second bi-polar transistor includes a second emitter region of the first conduction type, a second base region of the second conduction type, and a second collector region of the first conduction type, the second field effect transistor includes a second gate electrode layer, a source region of the second conduction type, and a drain region of the second conduction type, the second field effect transistor further including a first body region of the first conduction type formed at least between the source region of the second conduction type and the drain region of the second conduction type, the first body region of the first conduction type is electrically connected to the second collector region of the first conduction type, the source region of the second conduction type is electrically connected to the second collector region of the first conduction type, the drain region of the second conduction type is electrically connected to the second base region of the second conduction type, the first collector region of the first conduction type is electrically connected to the second emitter region of the first conduction type,

and the first gate electrode layer is electrically connected to the second gate electrode layer. As explained in paper #7, such a device is an obvious variation of the device disclosed by Wolf in view of the teachings of Zheng et al, and Schwank et al.

A. However, claims 2 and 3 each require the above described device in combination with a first electrode layer that continues to a side section of the first gate electrode layer and reaches the element isolation region, wherein the first gate electrode layer is formed in a manner to cross over the element forming region, the source region of the first conduction type is formed in a first region surrounded by the first gate electrode layer in a forming region of the first field effect transistor, the first electrode layer, and the element isolation region, the drain region of the first conduction type and the collector region of the first conduction type are formed in a second region surrounded by the first gate electrode layer and the element isolation region, the emitter region of the first conduction type is formed in a third region surrounded by the first gate electrode layer in a forming region of the first bi-polar transistor, the first electrode layer and the element isolation region, and the first body region of the second conduction type is formed at least below the first gate electrode layer in the forming region of the first field effect transistor, and below a part of the first electrode layer. Such a combination is neither disclosed nor suggested by the references of record.

B. Similarly, claims 4 and 5 each require the above described device in combination with a first layer and a second layer, wherein the first layer has one end section continuing to the first gate electrode layer or the second layer, and another end section

reaching the element isolation region, the second layer has one end section continuing to the first gate electrode layer or the second layer, and another end section reaching the element isolation region, the source region of the first conduction type is formed in a first region surrounded by the first gate electrode layer, the first layer and the element isolation region, the drain region of the first conduction type and the first collector region of the first conduction type are formed in a second region surrounded by the first gate electrode layer, the second layer and the element isolation region, the first emitter region of the first conduction type is formed in a third region surrounded by the first layer, the second layer and the element isolation region, the first base region of the second conduction type is formed below a part of the first layer, and below a part of the second layer in the semiconductor layer, and the first body region of the second conduction type is formed at least below the first gate electrode layer and below a part of the first layer in the semiconductor layer. Such a combination is neither disclosed nor suggested by the references of record.

C. Claim 6 requires the above-described device in combination with a second body region of the first conduction type, which is formed in the semiconductor layer between the first base region of the second conduction type and the first collector region of the first conduction type. Such a combination is neither disclosed nor suggested by the references of record.

D. Claims 7,8, and 10 each require the above described device in combination with an impurity diffusion layer of the second conduction type formed in the first element

forming region, wherein the impurity diffusion layer of the second conduction type is a semiconductor layer in the first region, and is formed in the semiconductor layer between the source region of the first conduction type and the first body region of the second conduction type, and the source region of the first conduction type and the first body region of the second conduction type are electrically connected to one another through the impurity diffusion layer of the second conduction type Such a combination is neither disclosed nor suggested by the references of record.

E. Claims 9 and 11 each require the above described device in combination with a third body region of the second conduction type is formed in the semiconductor layer between the first collector region of the first conduction type and the first emitter region of the first conduction type and in the semiconductor layer adjacent to the element isolation region. Such a combination is neither disclosed nor suggested by the references of record.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 703-308-0980. The examiner can normally be reached on Monday through Thursday 8 AM to 6 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers

for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 306-3431.

tld
05/2003

Minhloan Tran
Primary Examiner
Art Unit 2826